

FIG. 3

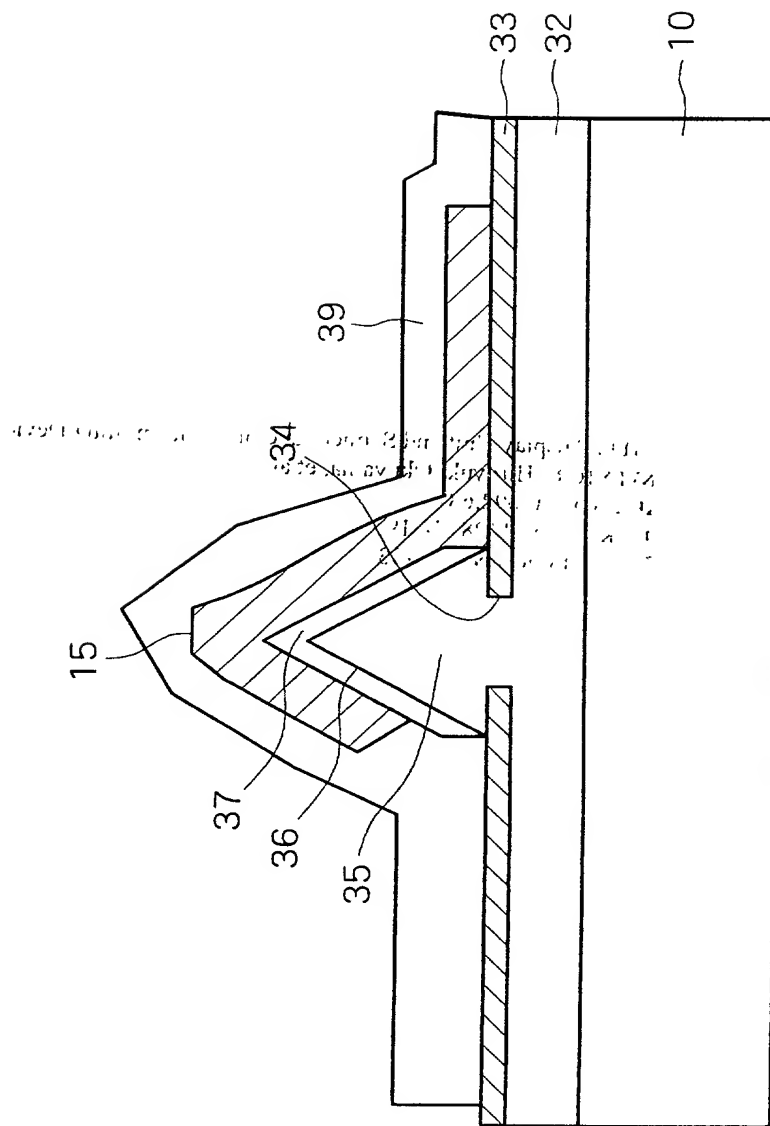


FIG. 4

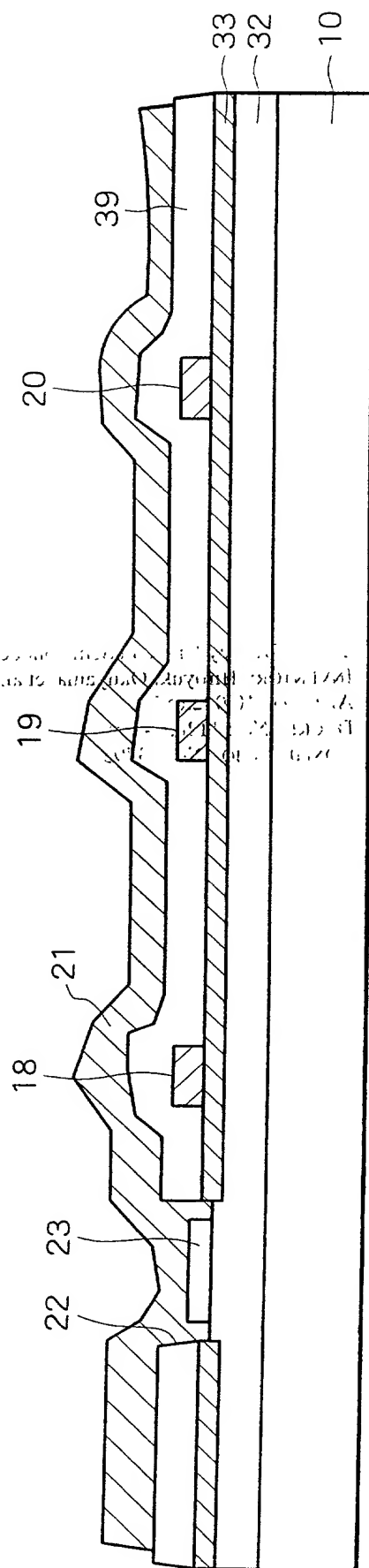
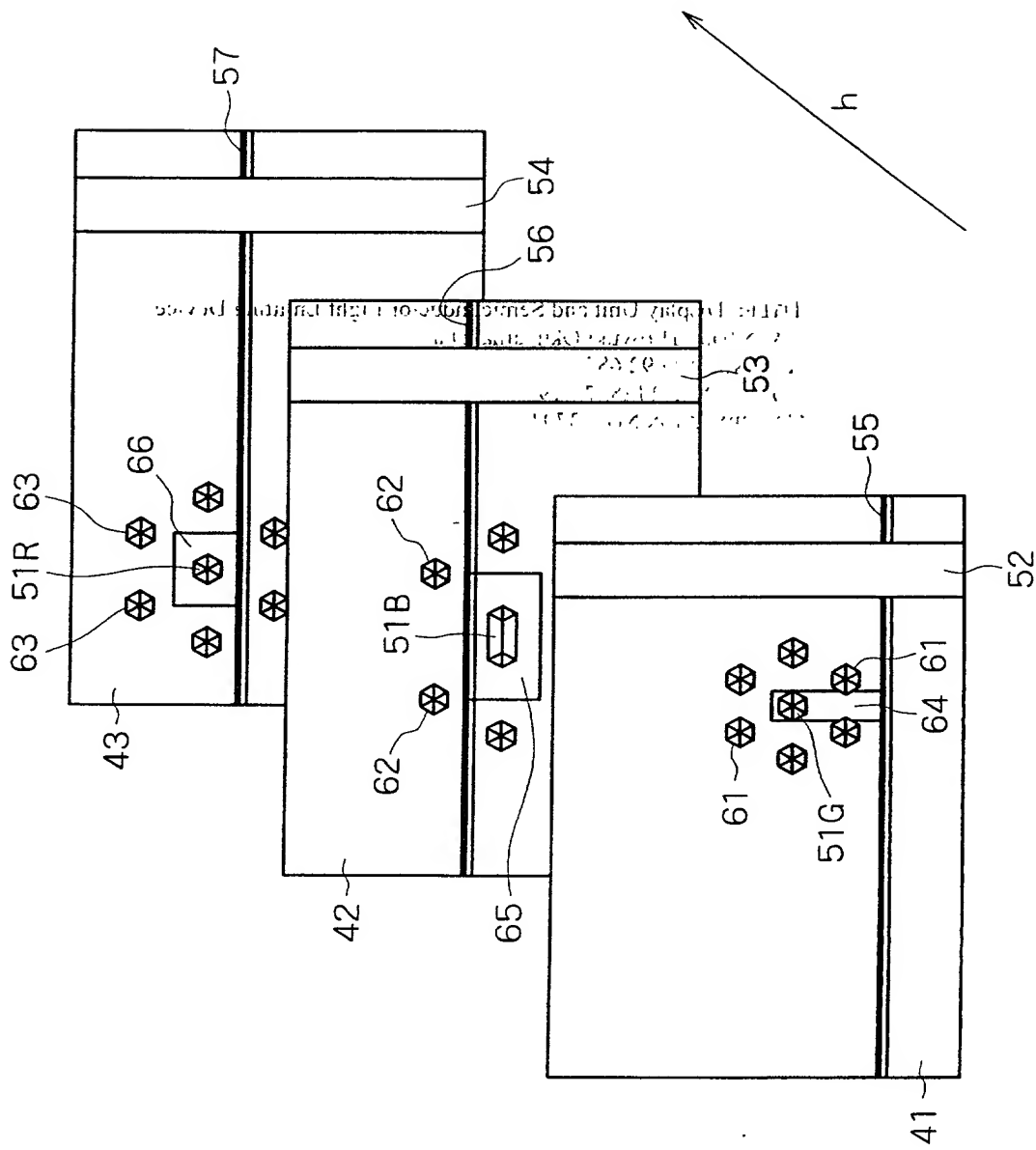


FIG. 5



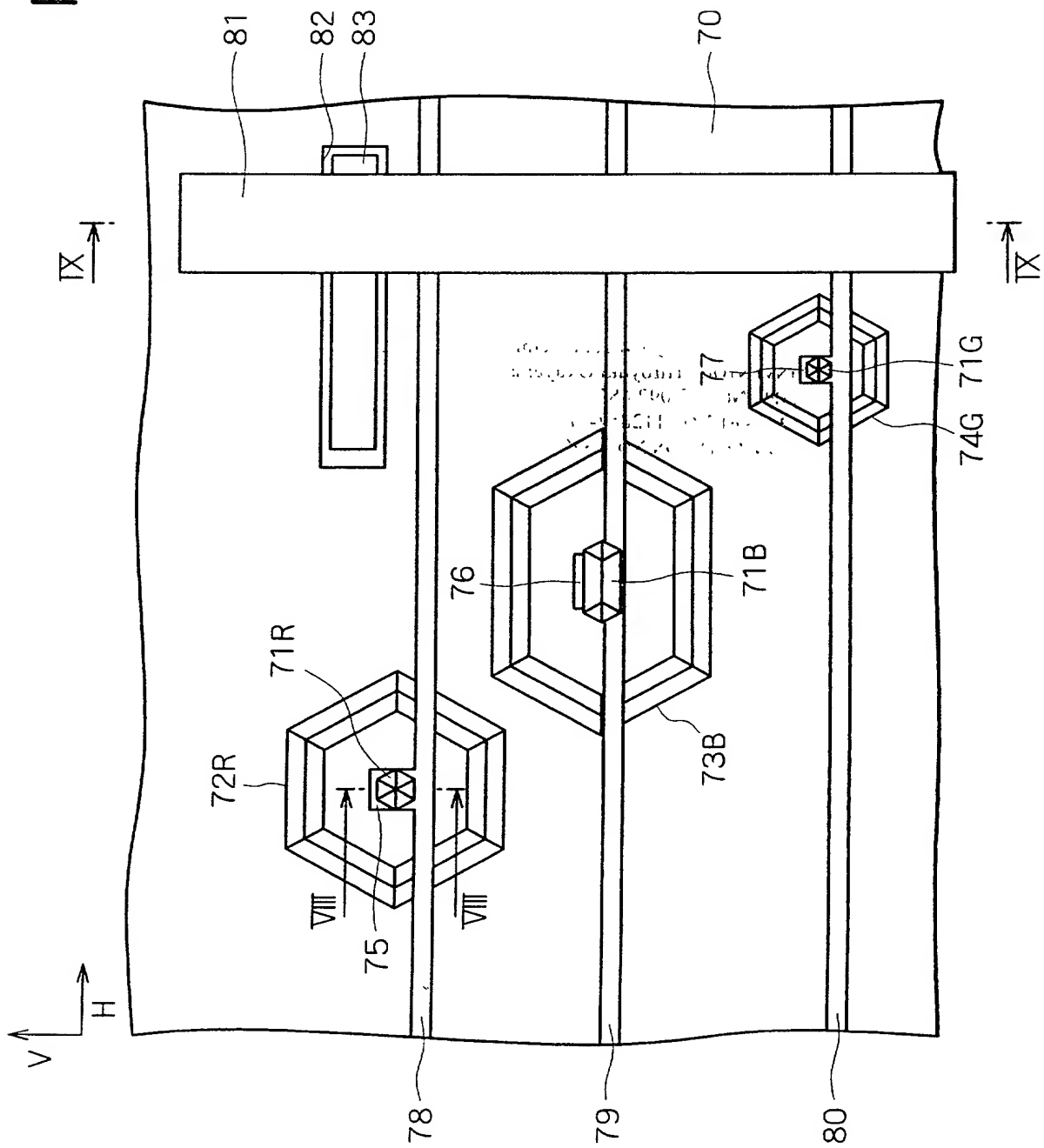


FIG. 6

FIG. 7

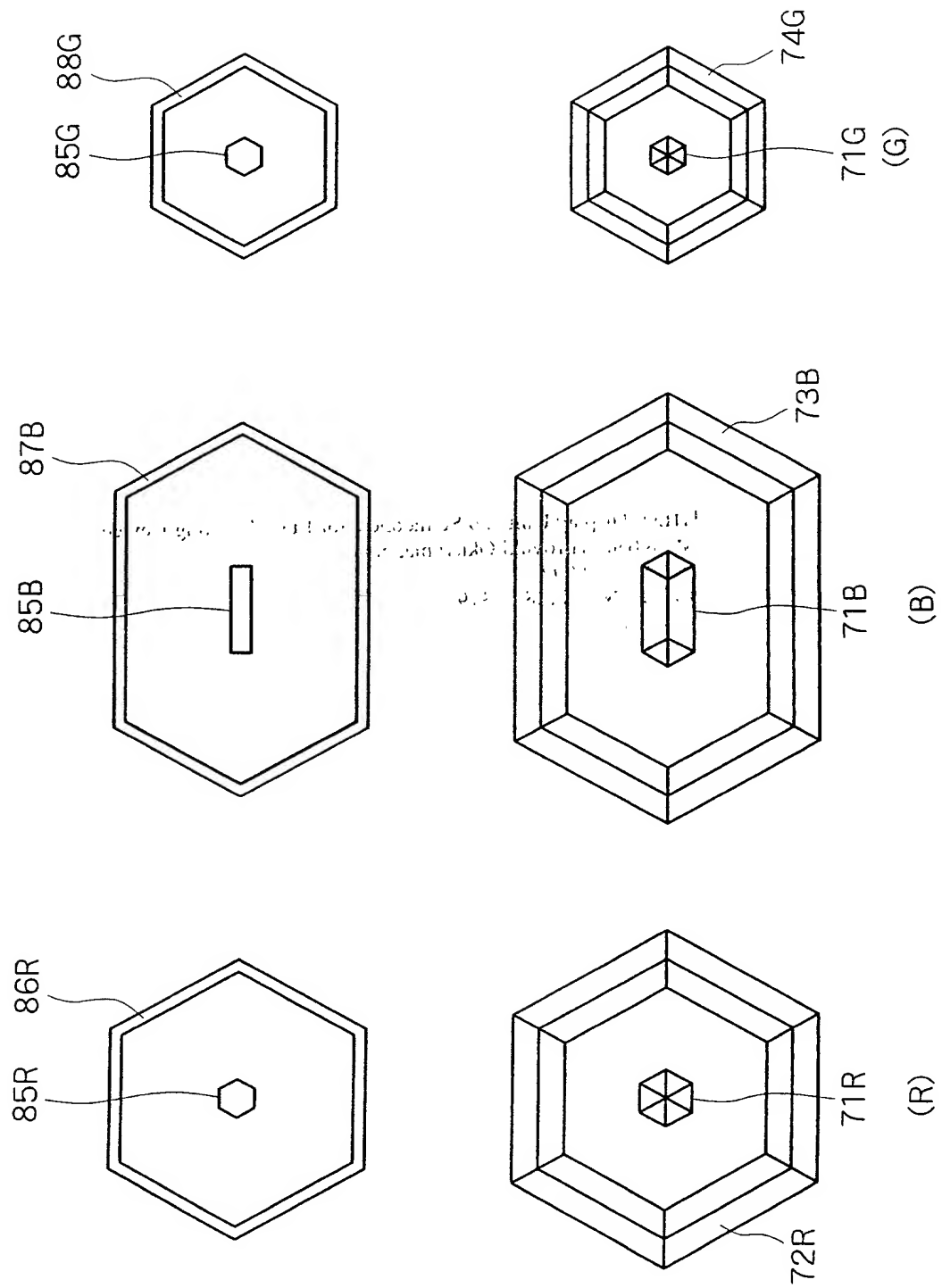


FIG. 8

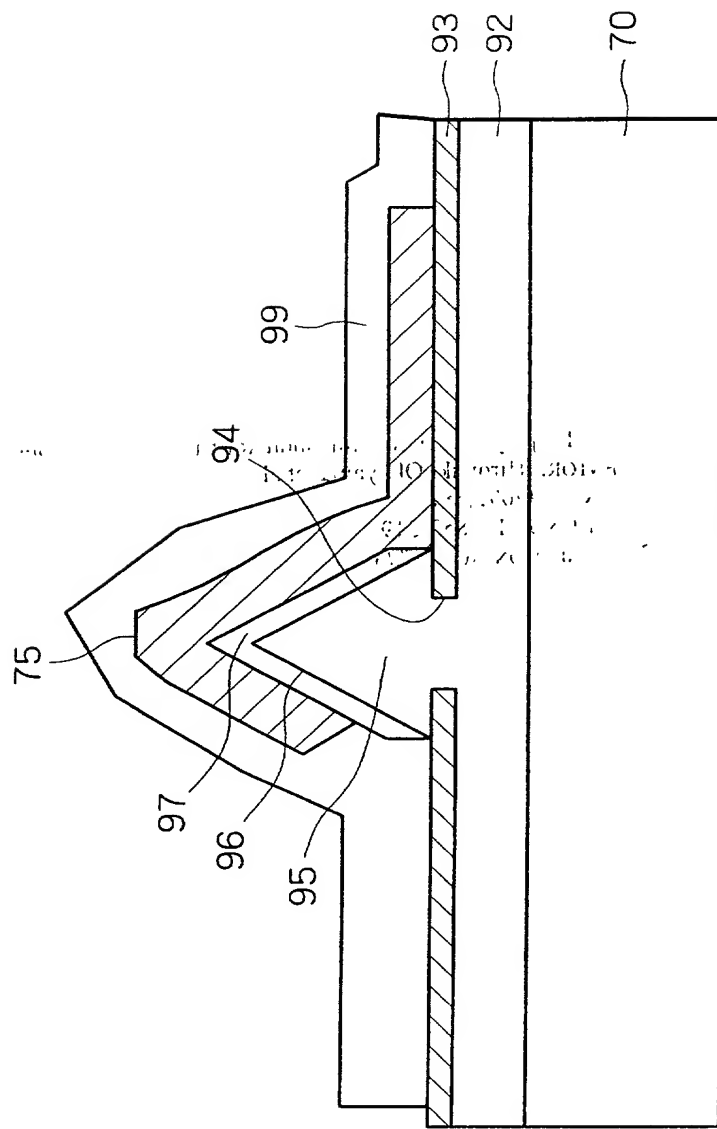
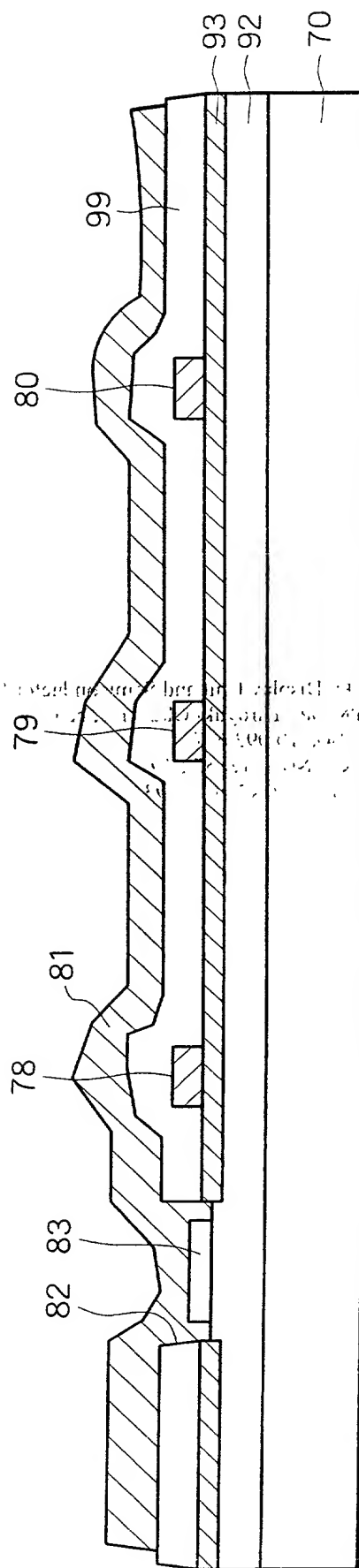
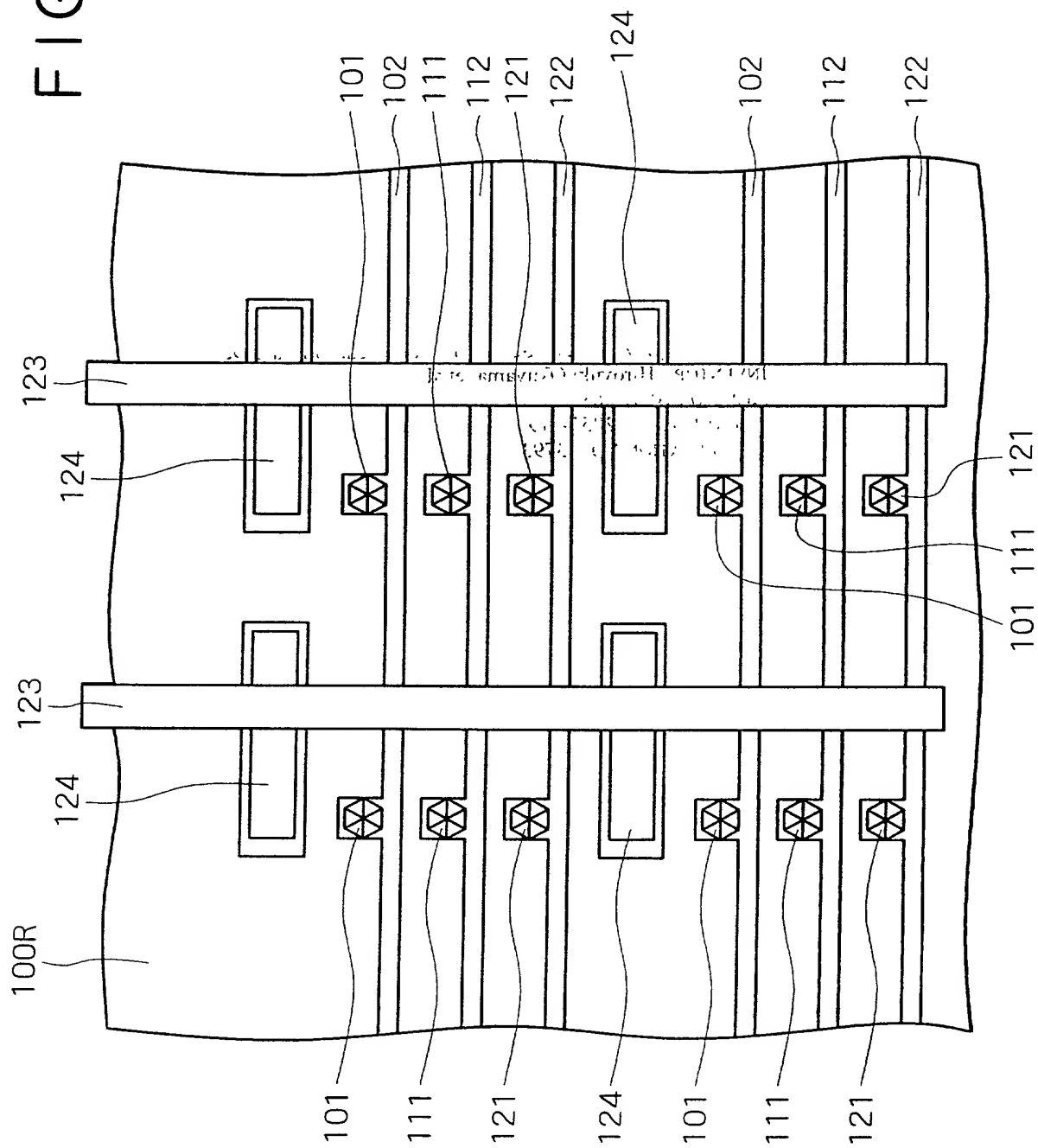


FIG. 9





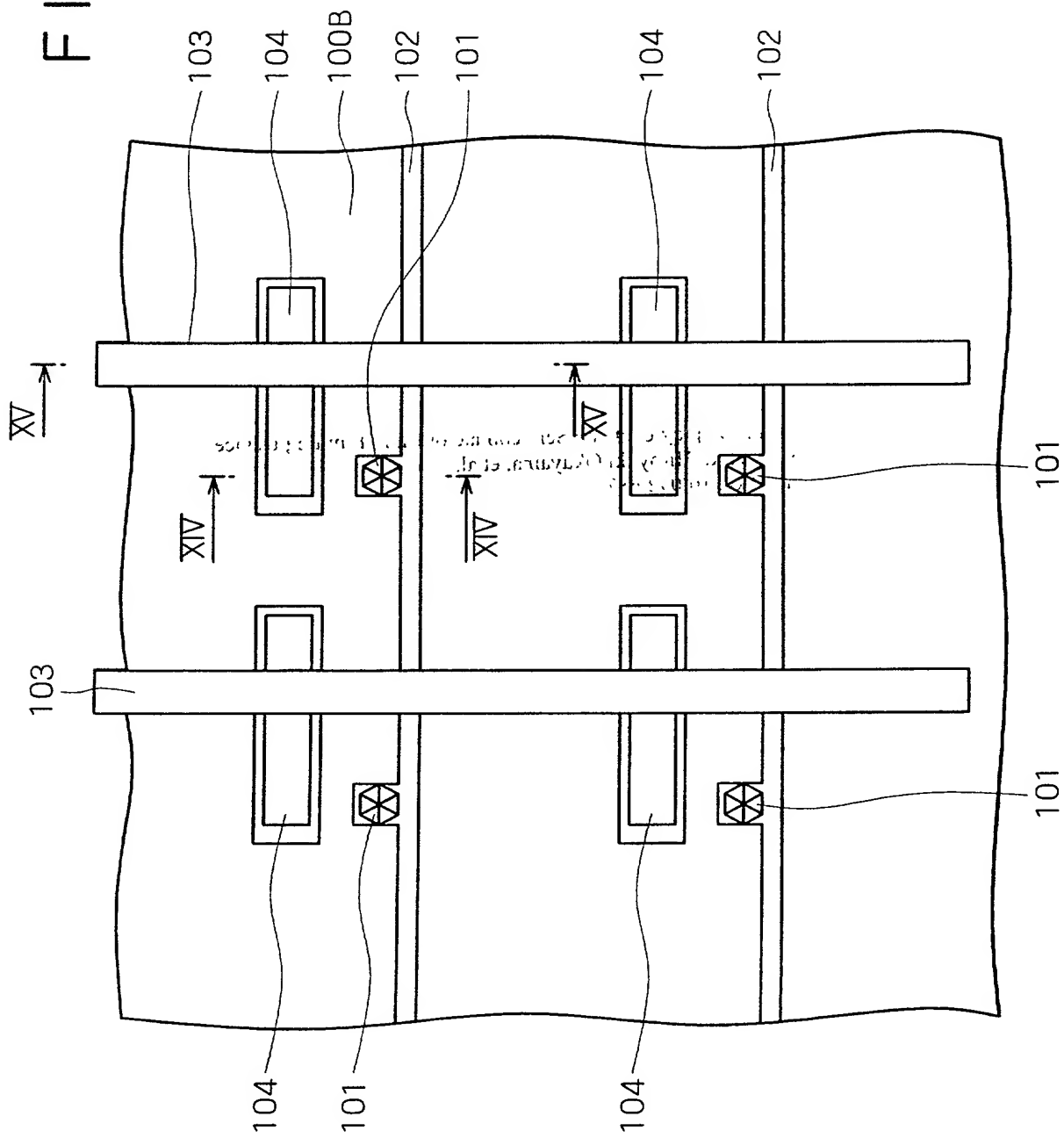


FIG. 11

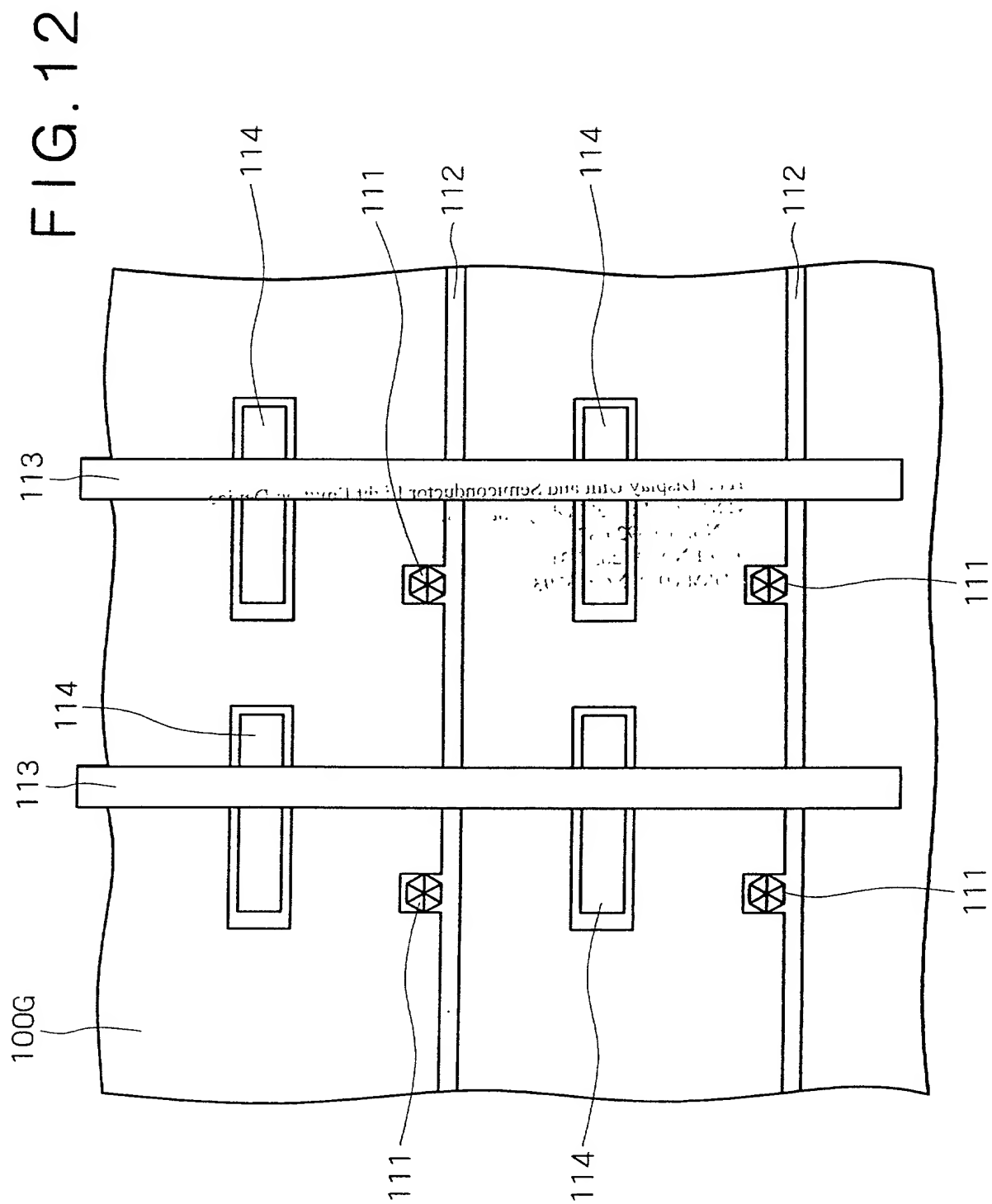


FIG. 13

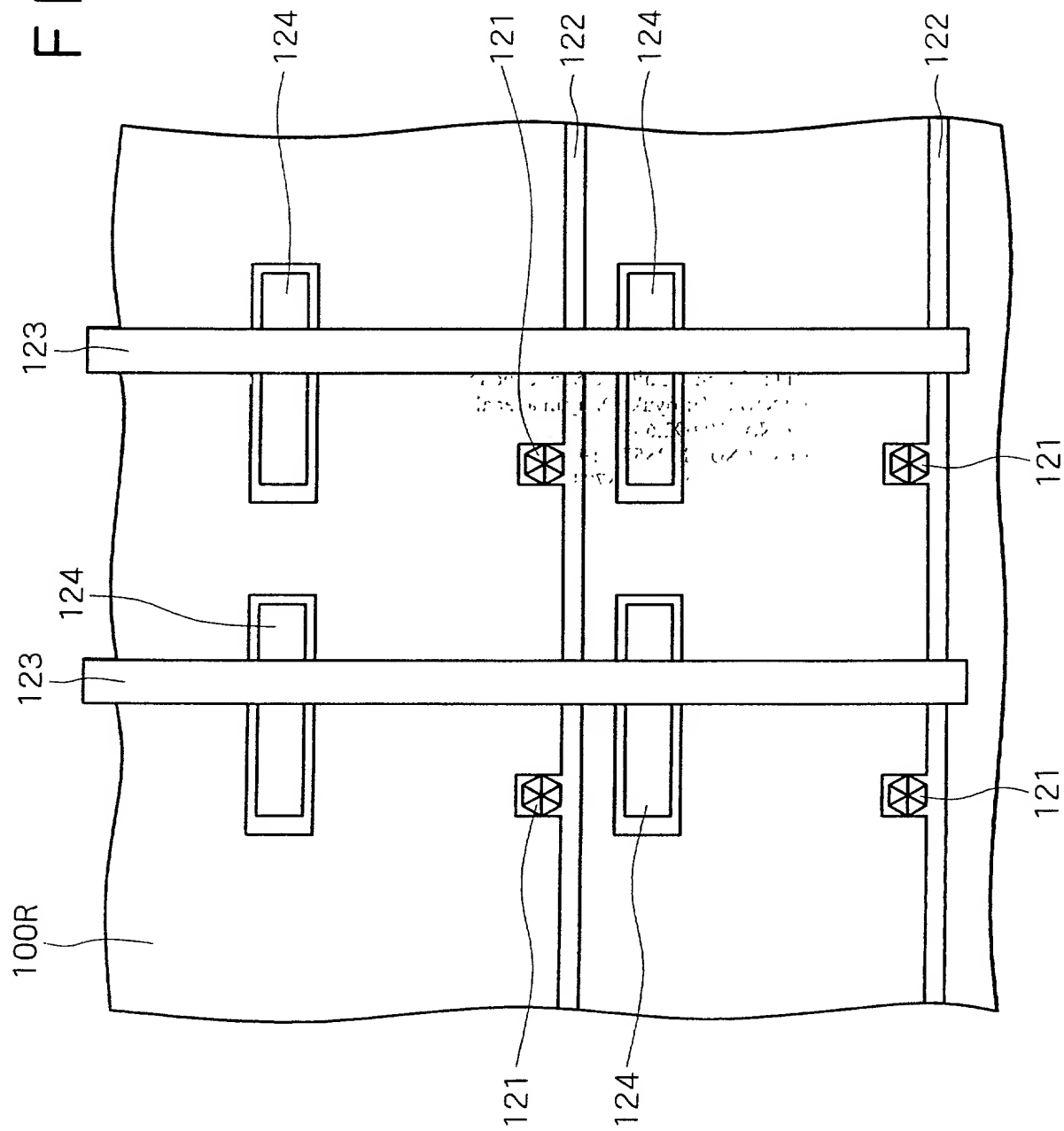


FIG. 14

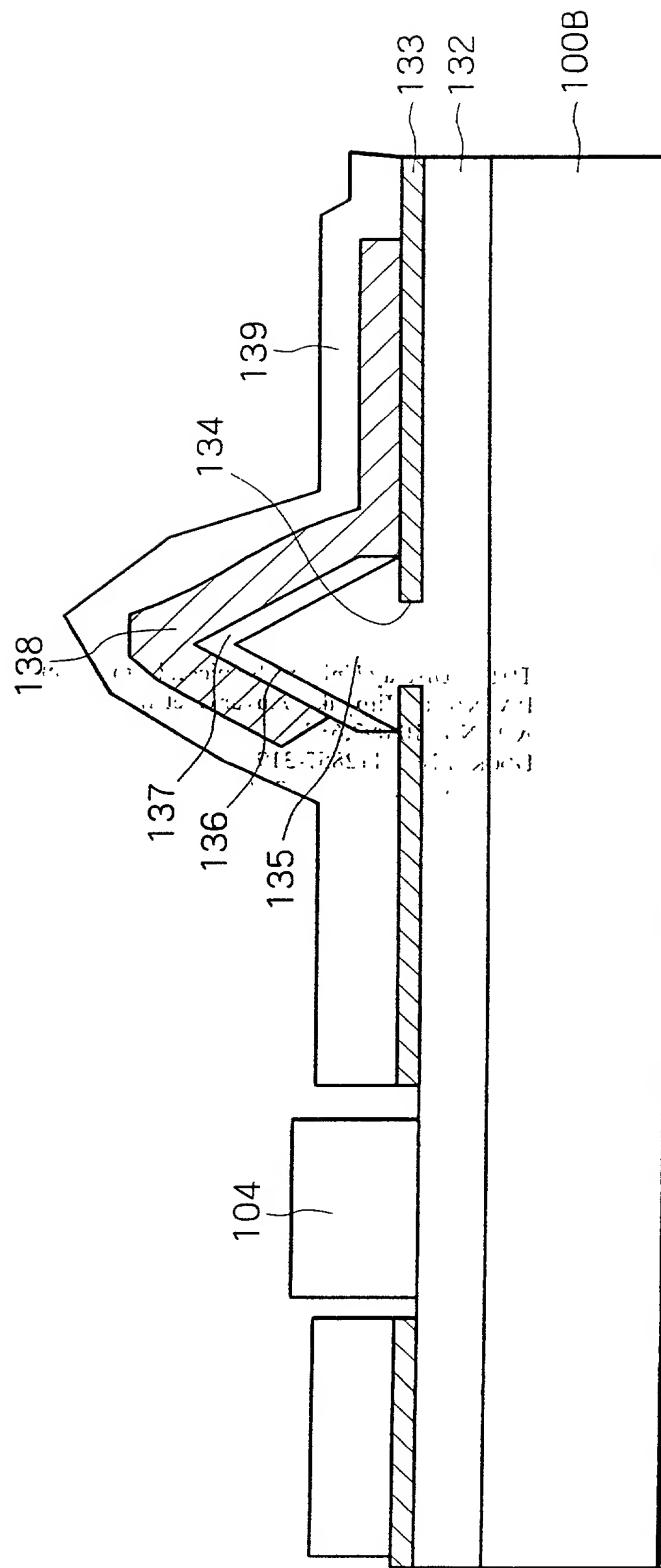


FIG. 15

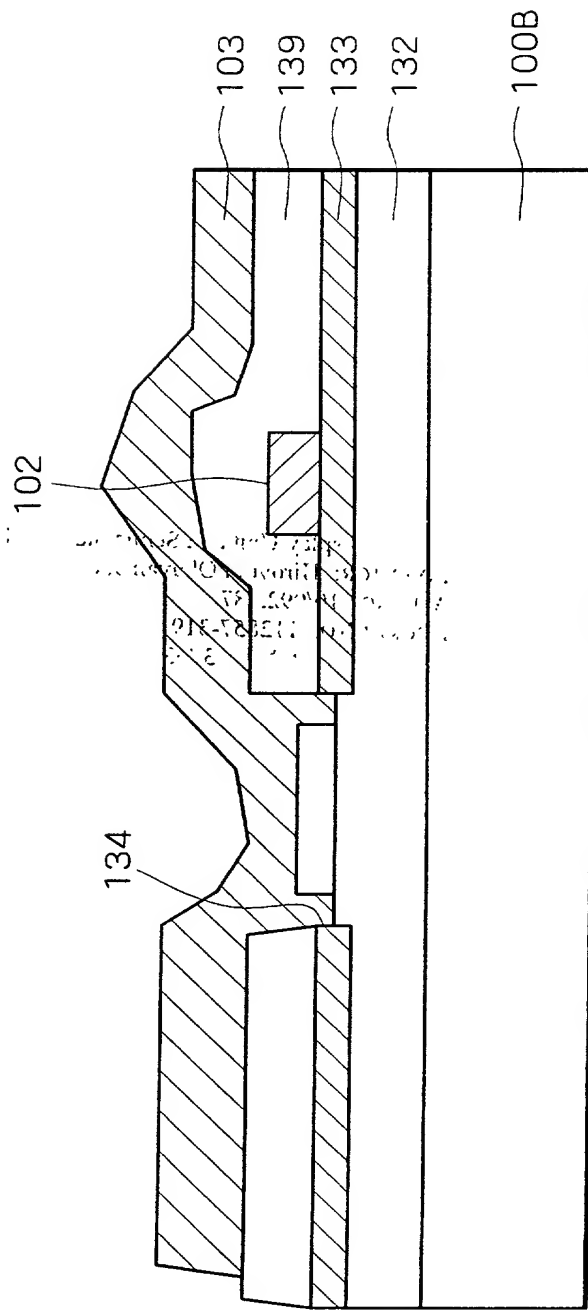


FIG. 16

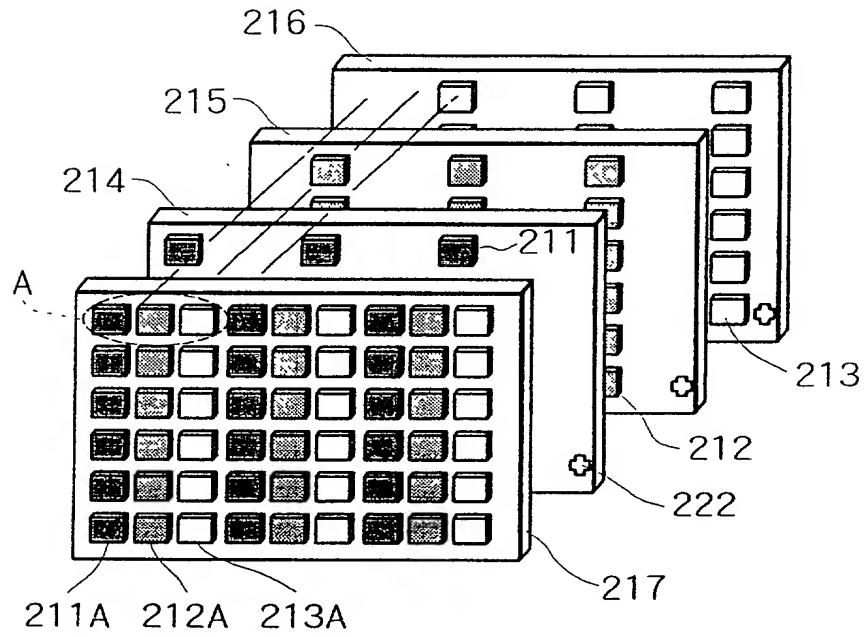


FIG. 17

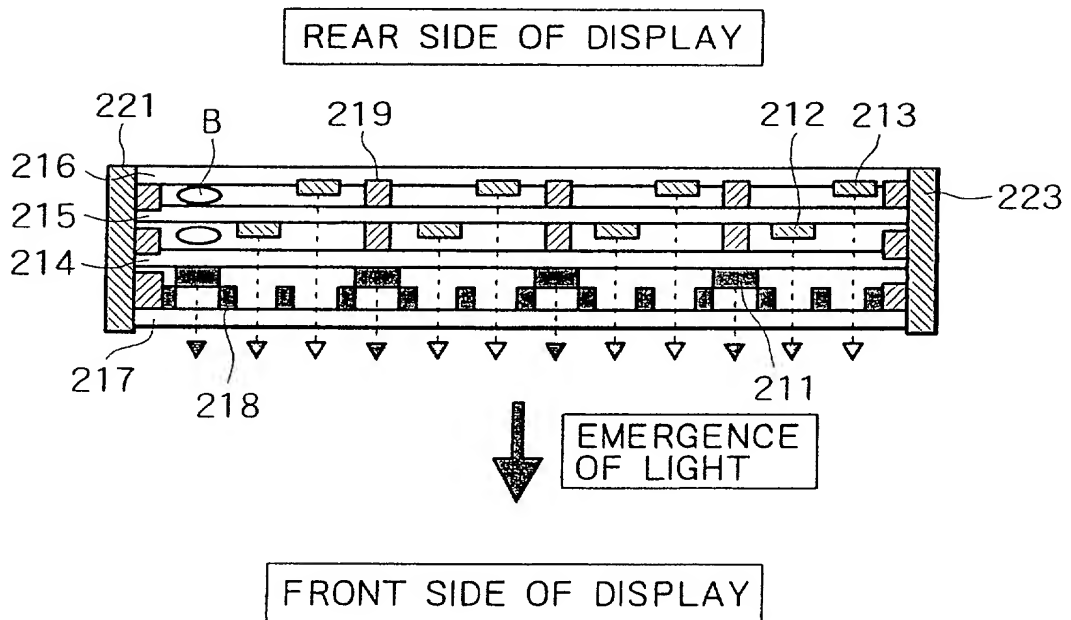


FIG. 18

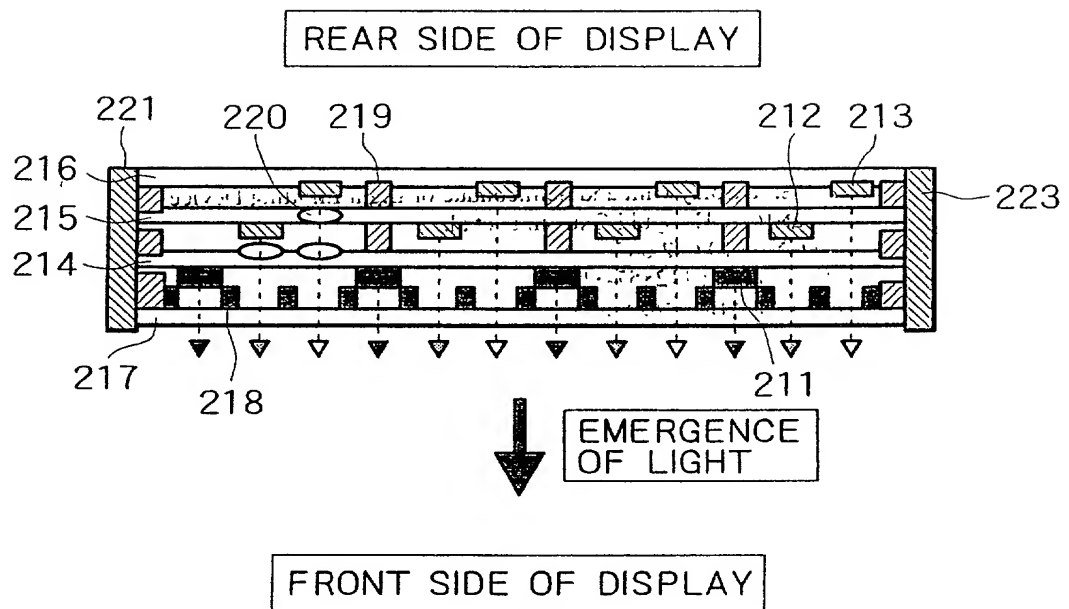


FIG. 19A

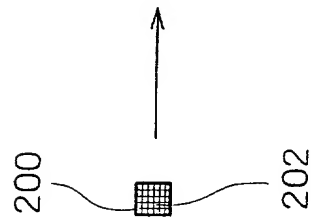


FIG. 19B

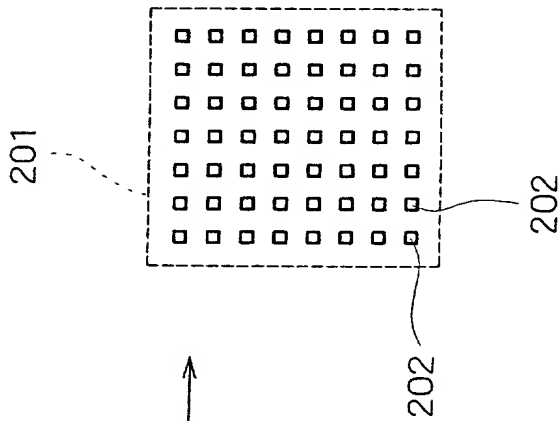


FIG. 19C

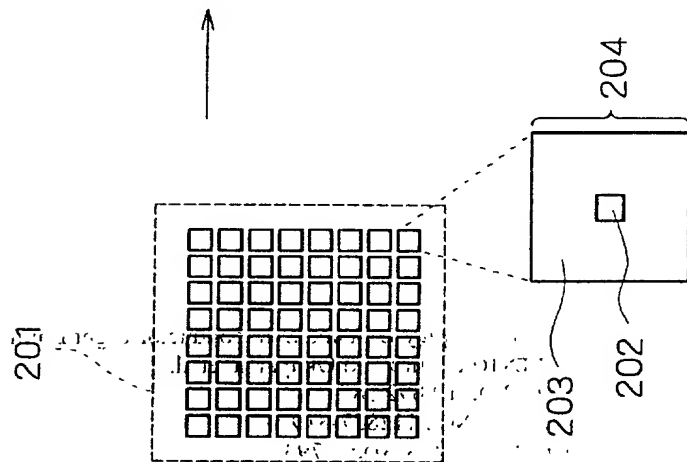


FIG. 19D

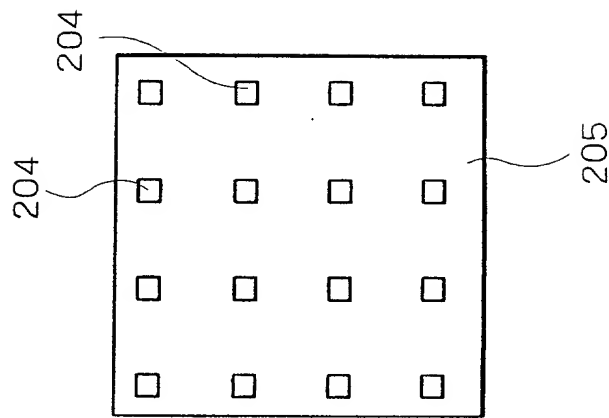


FIG. 20

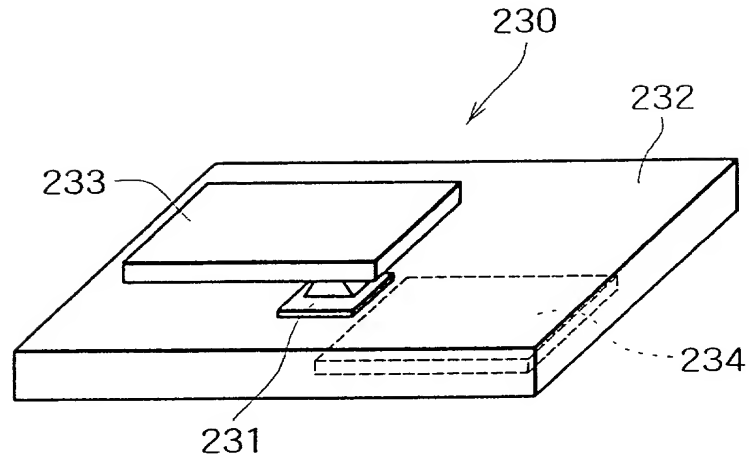


FIG. 21

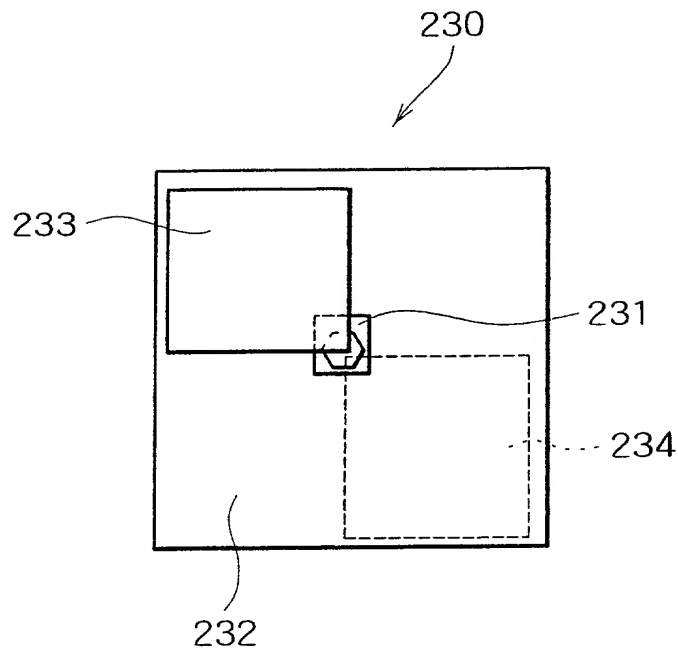


FIG. 22

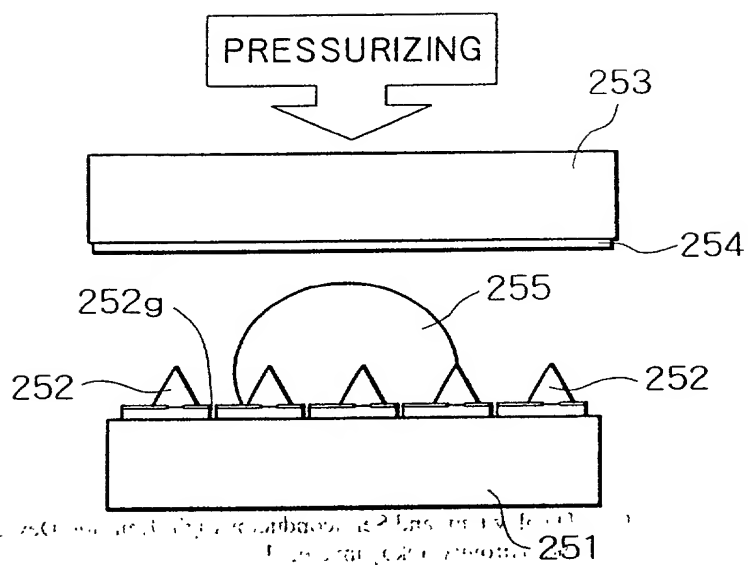


FIG. 23

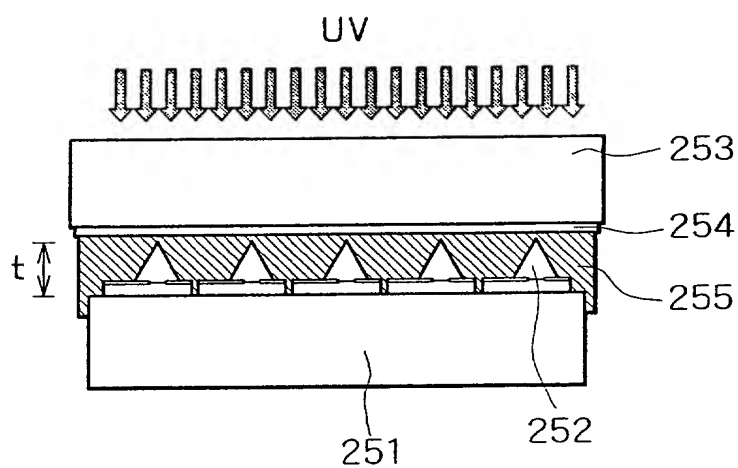


FIG. 24

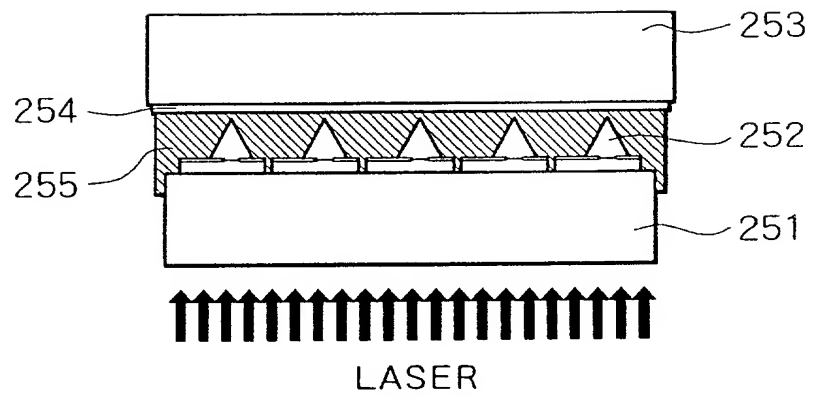


FIG. 25

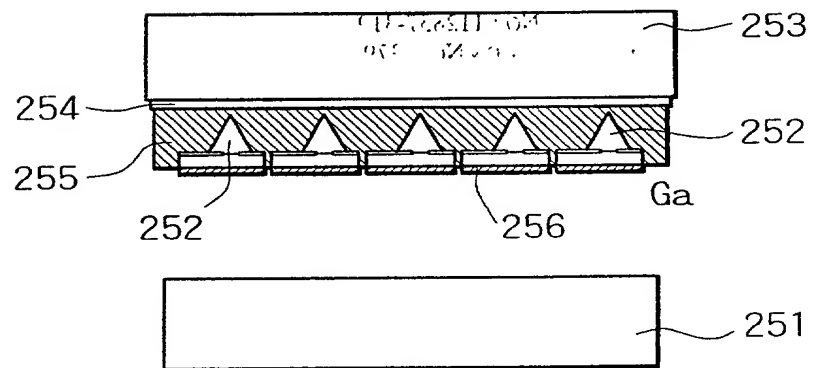


FIG. 26

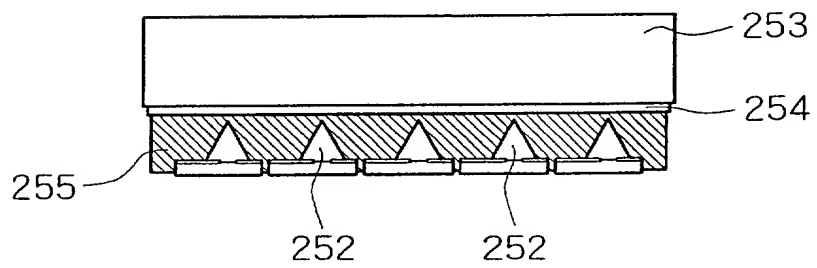


FIG. 27

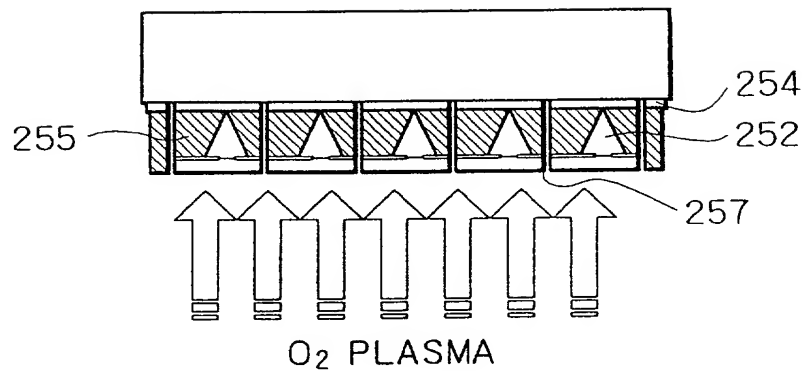


FIG. 28

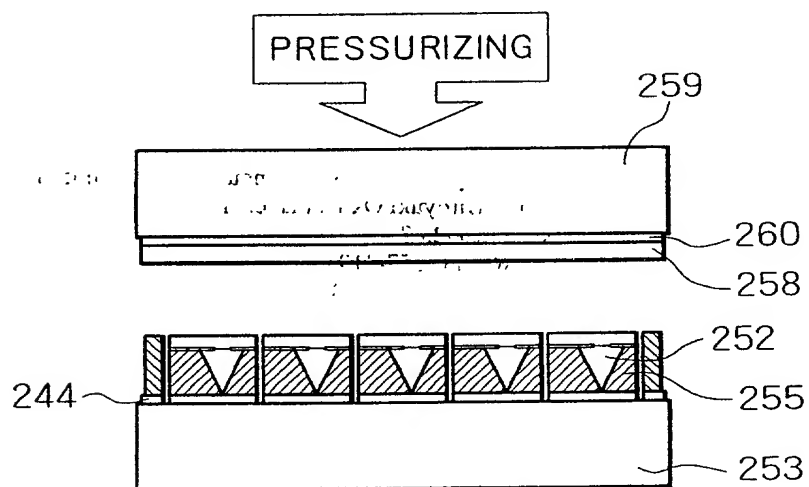


FIG. 29

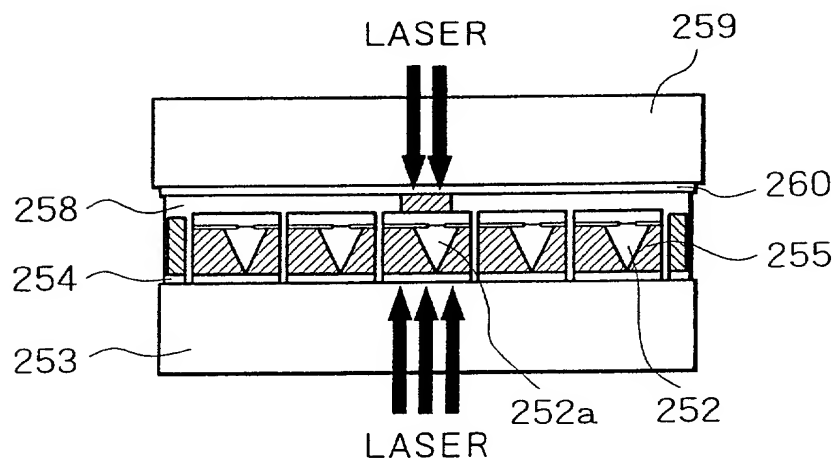


FIG. 30

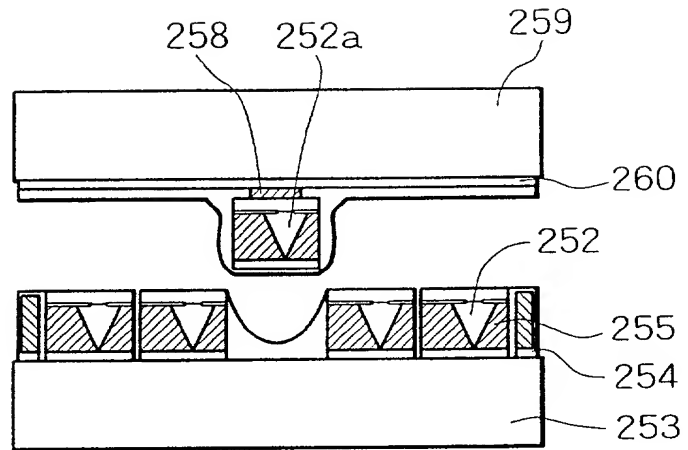


FIG. 31

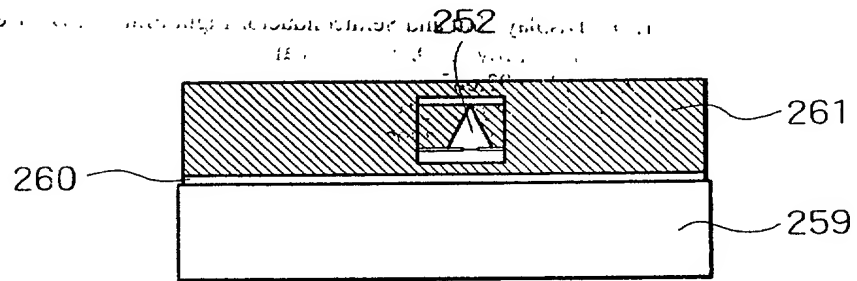


FIG. 32

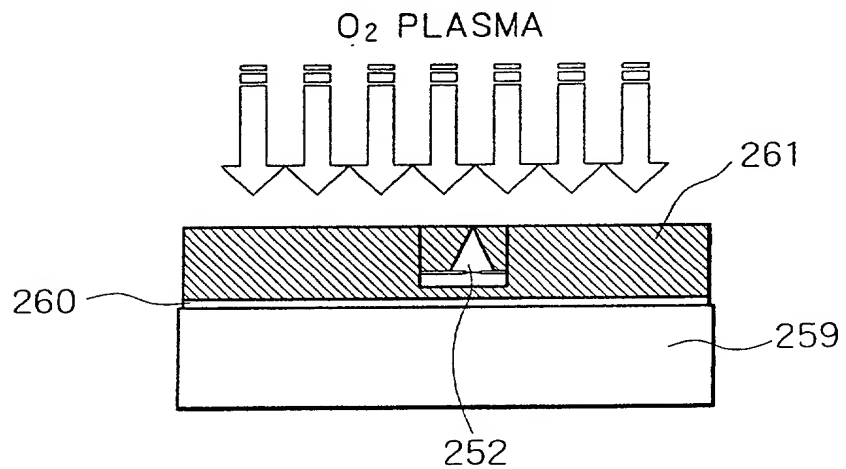


FIG. 33

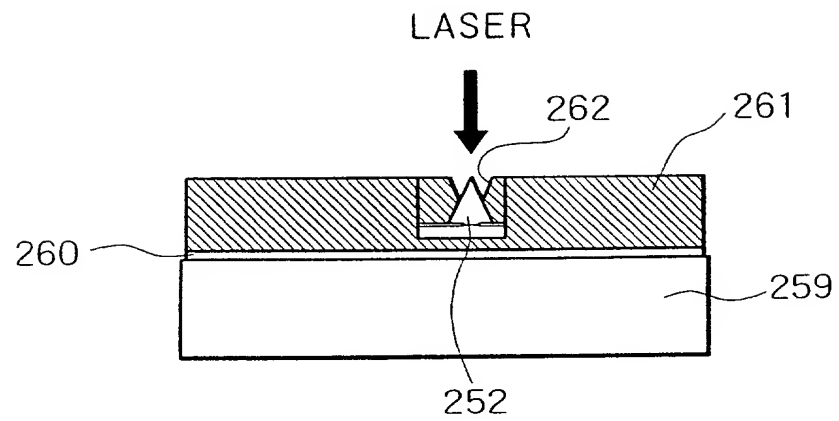


FIG. 34

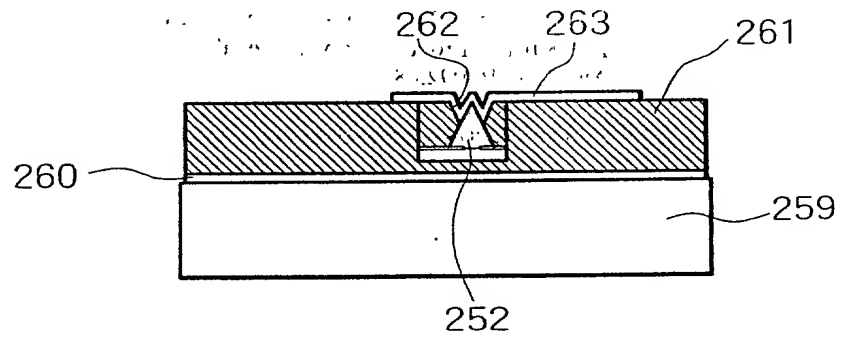


FIG. 35

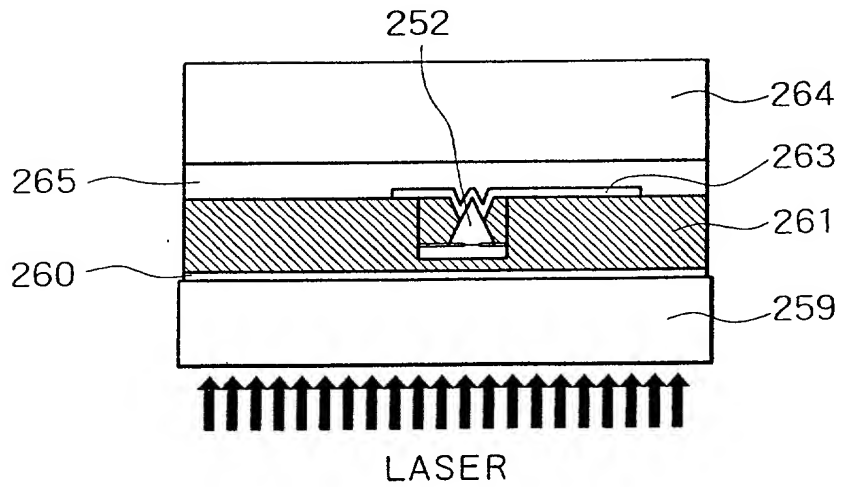


FIG. 36

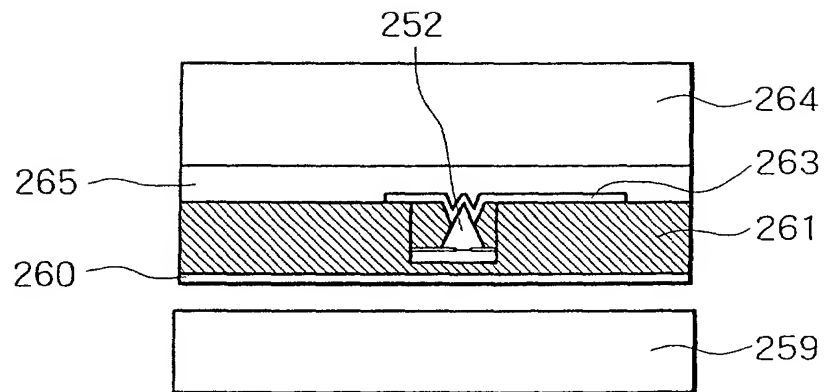


FIG. 37

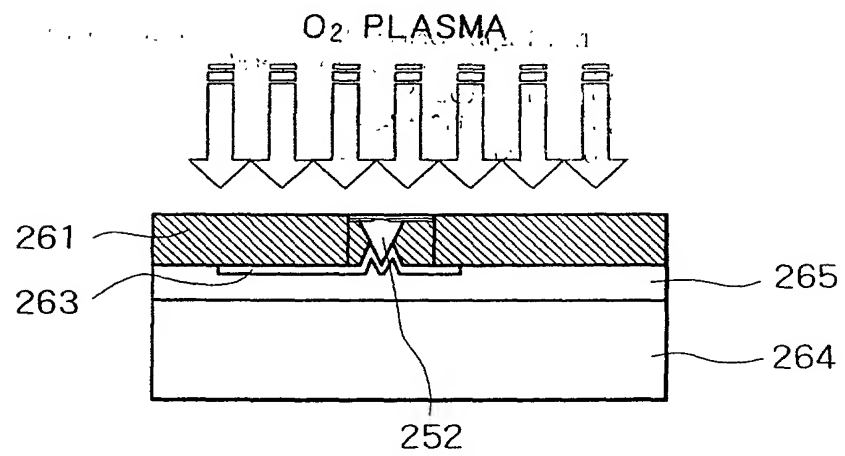


FIG. 38

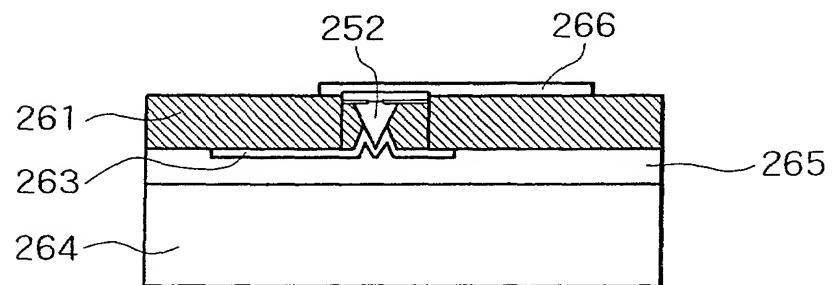


FIG. 39

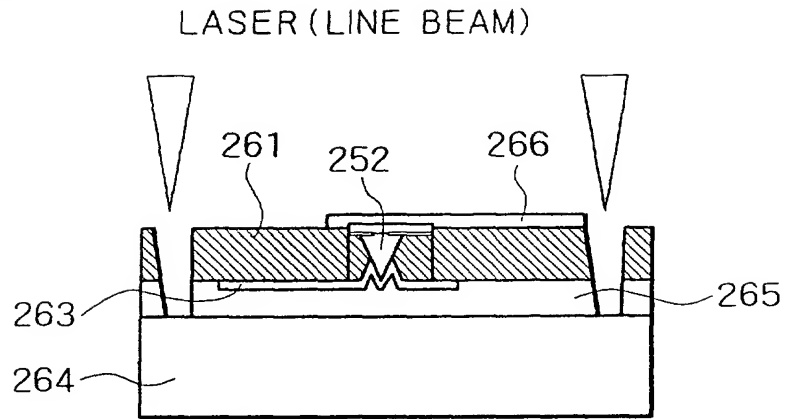


FIG. 40

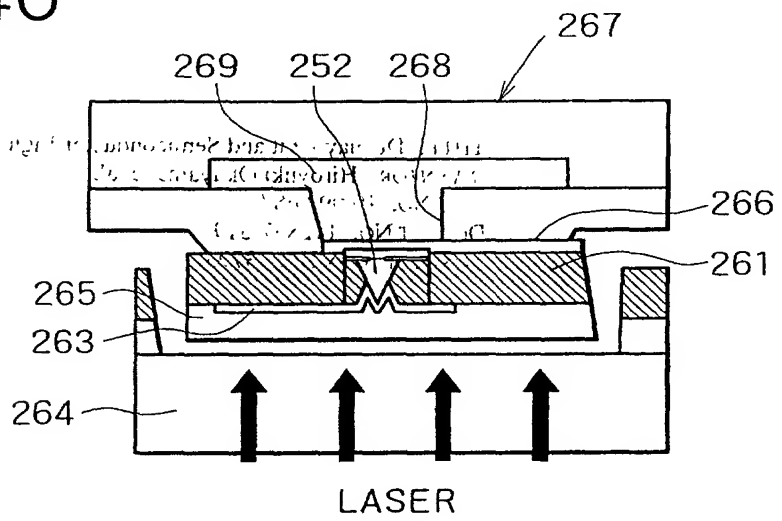


FIG. 41

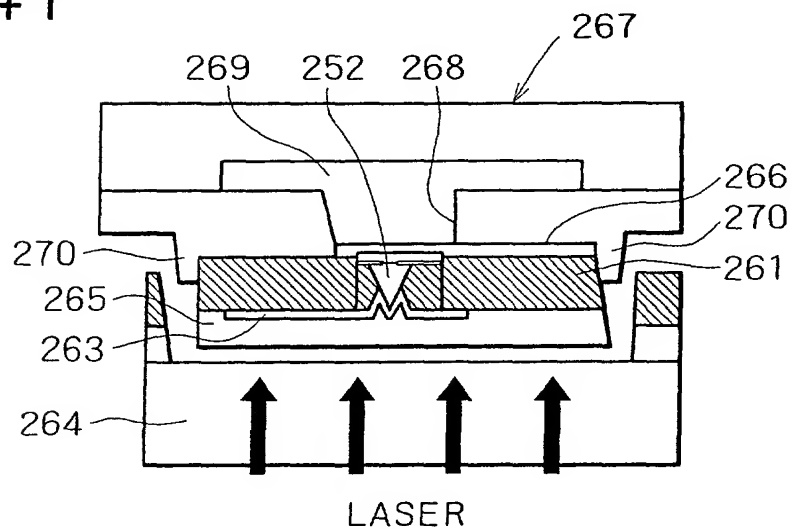


FIG. 42

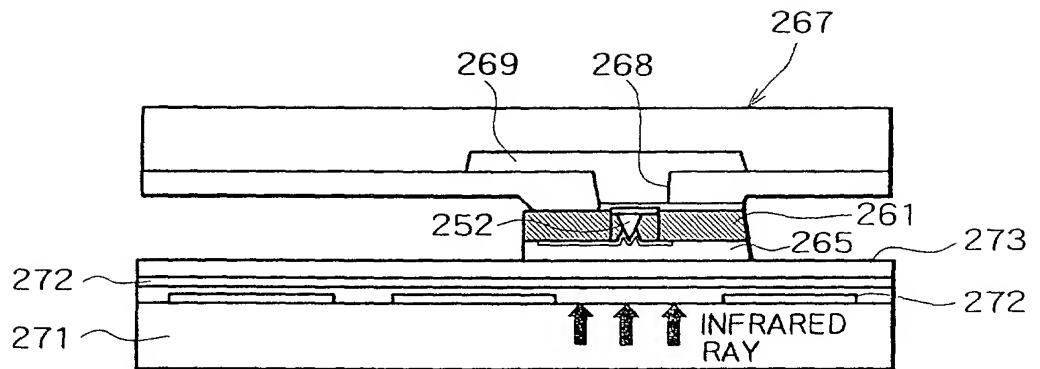


FIG. 43

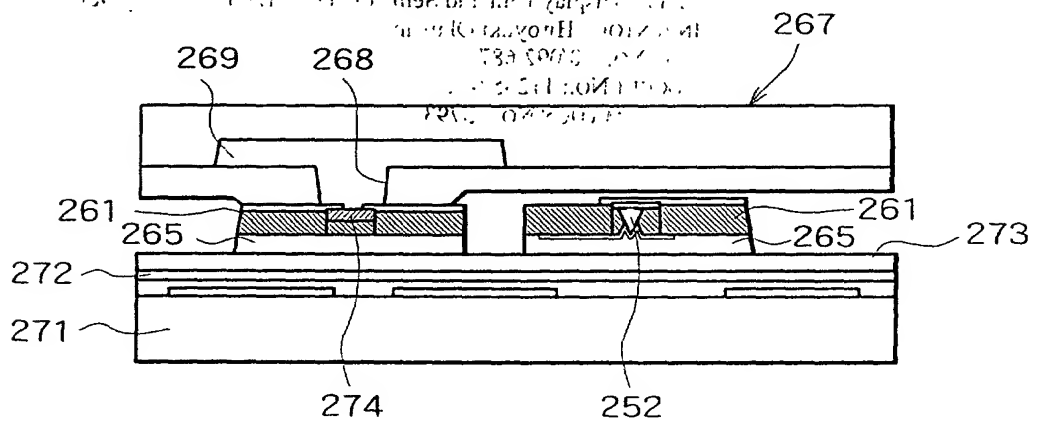


FIG. 44

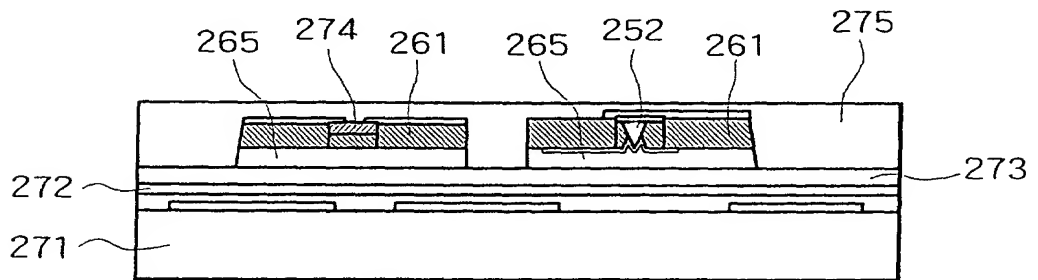


FIG. 45

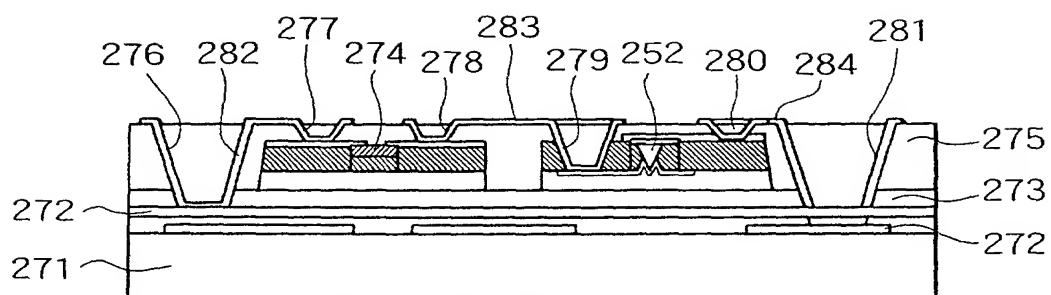


FIG. 45 is a cross-sectional view of a semiconductor device. The device includes a substrate 271, a layer 272, a patterned layer 273, and a top layer 275. The top layer 275 contains several rectangular features labeled 276, 282, 277, 274, 278, 283, 279, 252, 280, 284, and 281. The features 276, 282, 277, 274, 278, 283, 279, 252, 280, and 284 are filled with a hatched pattern, while feature 281 is empty.

FIG. 46

